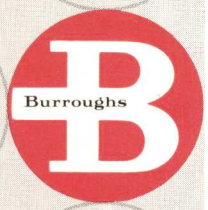
AN

TR 61-58B

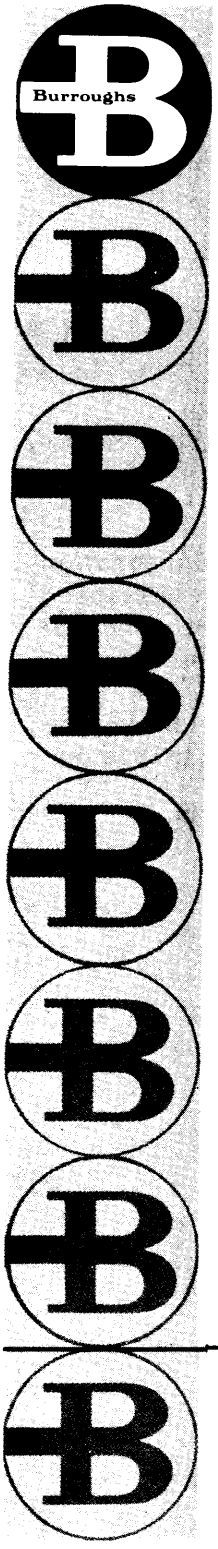


AN EXPANSIBLE, ULTRA HIGH SPEED,
GENERAL-PURPOSE COMPUTING SYSTEM

THE BURROUGHS D 825 MODULAR PROCESSOR SYSTEM

Burroughs Corporation

TR 61-58B



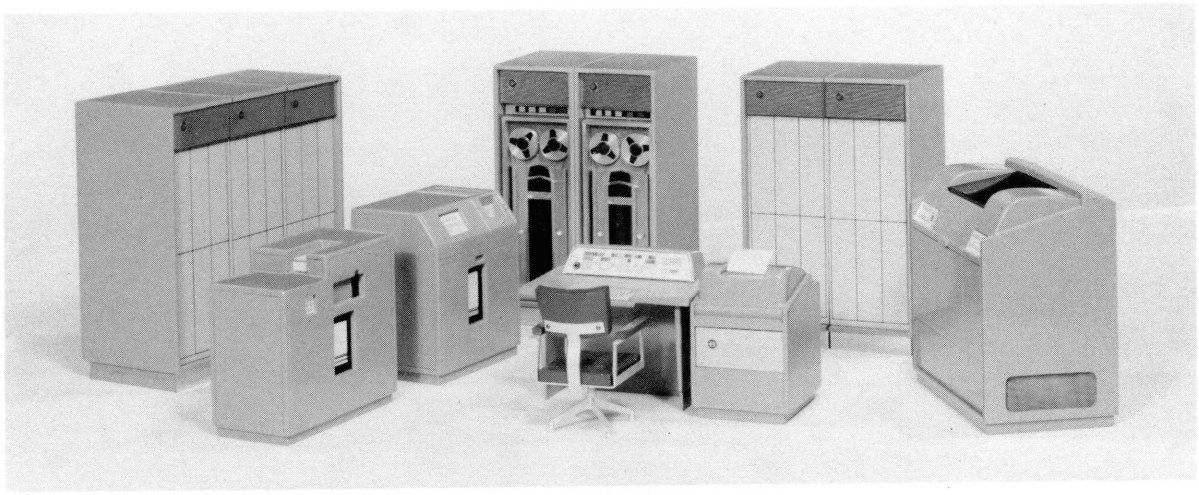
AN EXPANSIBLE, ULTRA HIGH SPEED, GENERAL-PURPOSE COMPUTING SYSTEM

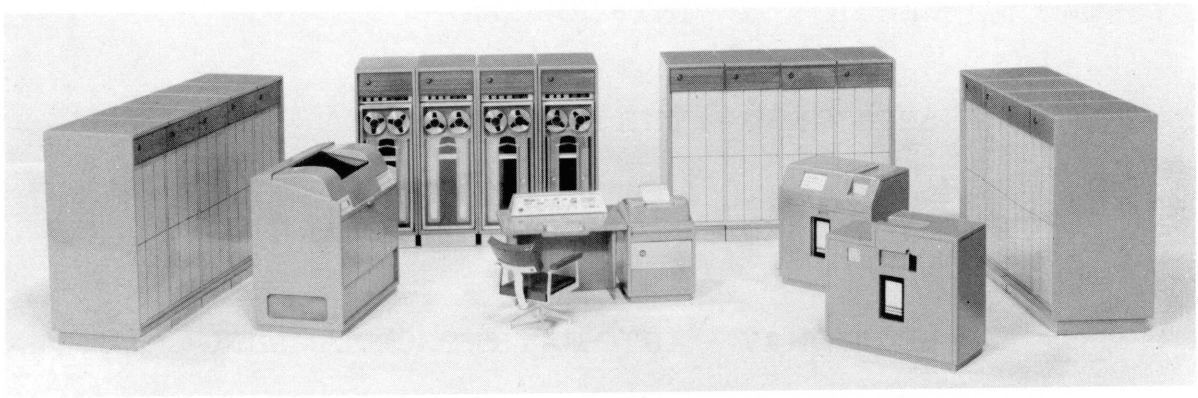
THE BURROUGHS D 825 MODULAR PROCESSOR SYSTEM

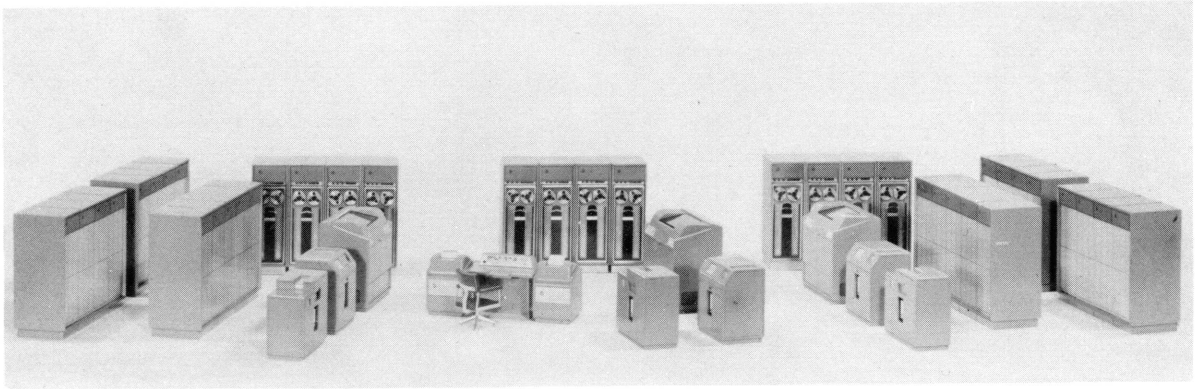
- DESIGNED TO MEET THE MILITARY ENVIRONMENT, EMPLOYING ADVANCED YET PROVED TECHNIQUES AND STANDARD COMPONENTS
- REAL-TIME, MULTIPROBLEM CAPABILITY
- GREAT PROGRAMMING FLEXIBILITY AND AUTOMATIC PARALLEL MODULE ASSIGNMENT
- EXCEPTIONAL RELIABILITY, SELF-DIAGNOSIS, AND AUTOMATIC FAILURE BYPASS
- BROAD EXPANSIBILITY IN THE FIELD
- GREATER COMPUTING SPEED THAN ANY COMPETITIVE SYSTEM

Burroughs Corporation

CONTENTS







SECTION I

INTRODUCTION

Only recently has our military establishment been involved in a complex strategic environment using weapons of advanced technology and presenting requirements for large scale computation and data processing. Here concepts of the modern digital computer have been employed in almost infinite form to provide the automation, rapid recognition and reaction, accuracy, reliability, and equipment maintainability demanded. Small computers have been used in mobile systems where size, weight, and power consumption are critical. Larger computers are found in ground- or ship-based applications where the emphasis is generally greater on the number and diversity of tasks performed, and upon the sheer quantity of data to be processed. Such computers will be found in command, control, and communication systems, in air surveillance and traffic control systems, in nuclear system control operations, and in weather data collection and reporting systems, to name just a few.

A brief review of existing and proposed large-scale computer applications in the military field yields some very interesting observations. Many computer applications are extremely similar, for example, in function, speed, capacity, type of data handled, manner in which employed, and reliability and maintainability requirements. In many cases, general-purpose commercial equipment is used, representing a compromise between initial system requirements, and the expense and time required for the development of a more desirable special-purpose system conforming to military specifications. The most significant observation of all, however, is that, with little exception, most large-scale computer system installations become saturated with an

ever-increasing work load never contemplated during the system inception.

This growth in computing system workload is a natural evolutionary process which can usually be anticipated, but which can neither be suppressed nor completely predicted. To satisfy the changing needs of dynamic applications and to provide efficient data processing capability of maximum utility in this environment there has appeared a new concept of computer system organization which effectively marks the arrival of a second generation in computers: expansible modular computer systems which provide real-time processing flexibility.

A modular computer system, as the name implies, is a computer system made up of interconnected functionally independent modules such as computer modules, memory modules, input/output control modules, and so forth. Interconnection is made through a program-responsive switching matrix. Modules may be added as requirements grow. The system may be programmed to automatically assume an optimized working configuration for any problem or set of problems.

Such a system is the Burroughs D825 Modular Processor System. The system concept and details of the system modules are presented in Sections II and III respectively. Automatic programming is discussed in Section IV.

The Burroughs D825 Modular Processor System represents an effective solution to most large-scale ground-based military computing applications commensurate with modern, yet proved, computer techniques and components. This system approximates the capability and efficiency of a custom-tailored system through the use of a flexible organization of standard modular elements. The Burroughs approach has the additional advantage of built-in growth potential; the D825 Modular Processor System is independently expansible in effective computation speed and input-output capability, as well as in memory capacity, thus matching the innate growth proclivity of almost all data processing applications. This growth can be effected in the

field within the maximum configuration specified for the D825 system. Growth beyond this size is also practical. Addressing capability for a memory of 65,536 words is built into the system, and the unitized structure of the system data busses and data flow control (switching interlock) make system expansion to accommodate more memory, computer, and/or input-output control modules a relatively straightforward engineering task.

The D825 Modular Processor System is a 3-megacycle, synchronous, digital computing and data-processing system. Arithmetic processes and data flow within the system are serial-parallel in nature. The command structure of the computer includes binary, and alphanumeric instructions. Binary arithmetic may be fixed- or floating-point with the computer organization oriented toward efficient floating-point computation.

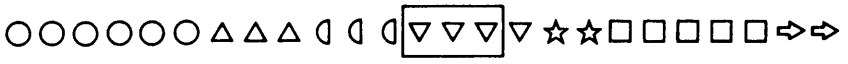
SECTION II

THE D825 CONCEPT

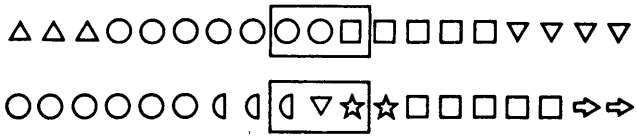
The D825 Modular Processor, the result of a two-year study by Burroughs of techniques for parallel processing and automatic programming, represents a totally new approach to computer organization, the first totally modular computing system. Adaptable to a wide range of computing applications, the D825 is broadly expansible in computer, memory, and input/output complements. The system schedules itself, ensures its own maximum efficiency, adapts to changes and growth in its workload (without reprogramming), diagnoses and automatically bypasses its own malfunctions, and cannot be totally disabled by any single failure of a system element. The D825, implemented with advanced techniques proved by Burroughs in military use, far exceeds all other computing systems in speed, expansibility, adaptability, flexibility, and reliability.

The D825 represents an evolutional step beyond conventional computer organization, an operational structure conceived and developed by Burroughs to provide a computing system which can be freely organized and freely expanded, using combinations of modular elements, to satisfy changing system requirements. The relationship of the D825 to previous system organization may be illustrated by considering the aspects of program time flow. Each group of symbols in the accompanying diagrams represents a program; program segments indicated by the individual symbols are occasionally repetitive. Time flow is from left to right; the computation rates and the workloads supplied are assumed to be equal.

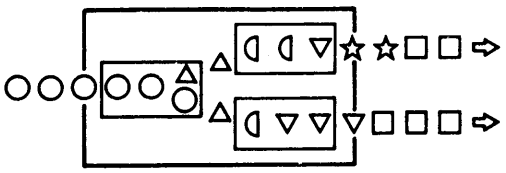
This configuration, the single-computer system, attacks a set of programs serially; program 1 is followed by program 2, and so forth.



When a point is reached where the computing capacity is saturated; the total program load cannot be run in the time available. The most obvious solution to the problem of system saturation is the brute force approach—simply add more computers and divide the workload. If individual programs in the workload are more or less unrelated, this approach, a multicomputer installation, is quite effective, and has, in fact, been exploited in many variations.

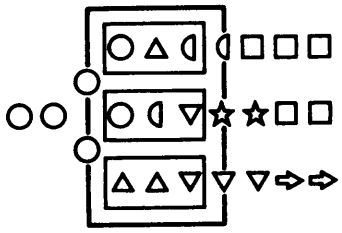


To make more effective use of the computing power available, the scheduling task can be performed by a master computer which assigns program segments in efficient patterns and sequences to a number of subservient computers.



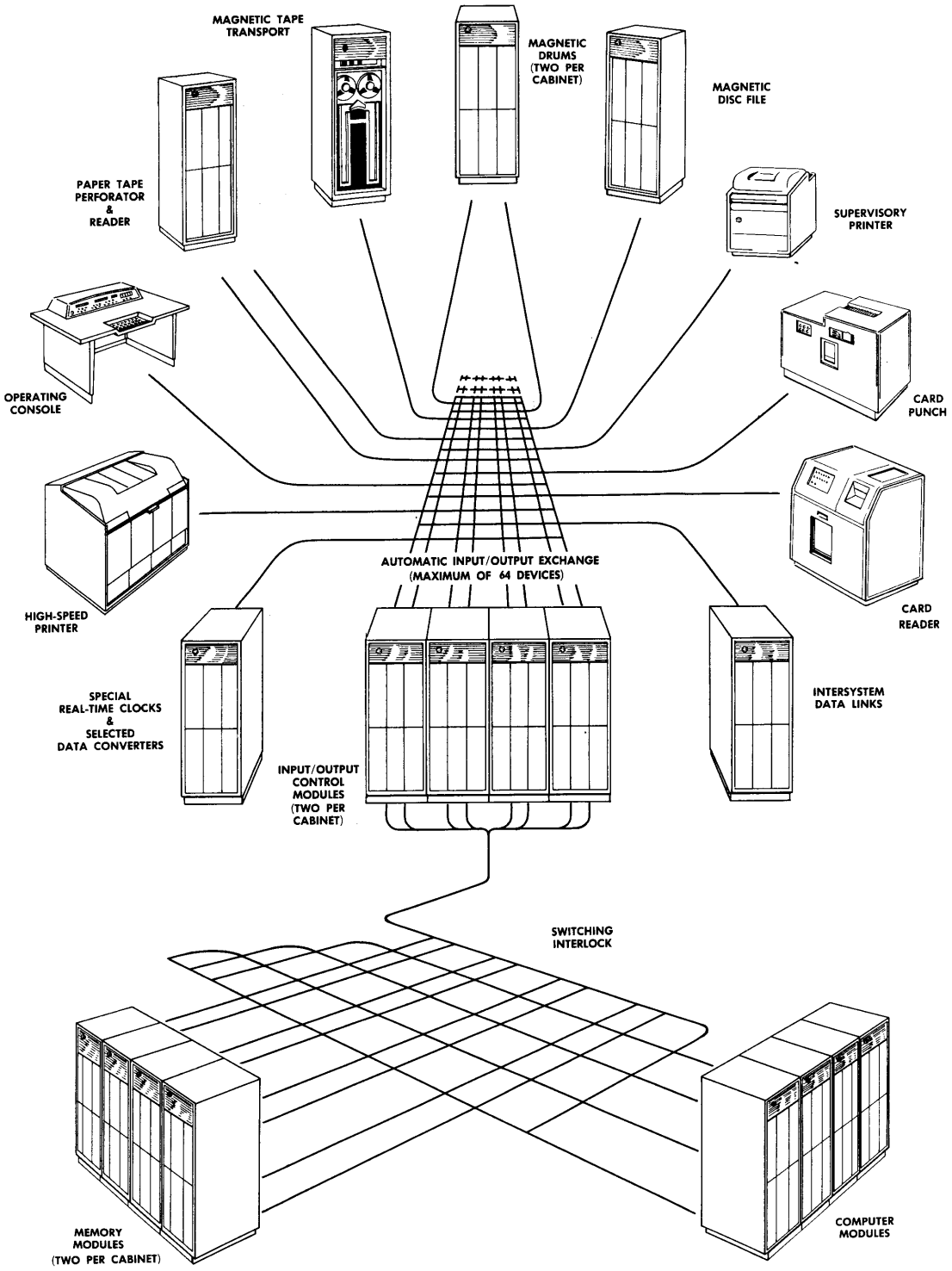
The semimodular computing system eliminates one source of efficiency but introduces a complex specialized element which works only part time. More significant for many applications is the vulnerability introduced; a failure in the master computer disables the entire system.

These shortcomings are overcome in the totally modular computing system. This approach, the ultimate in digital computer organization, was conceived and developed by Burroughs as the basis for the D825 Modular Processor. A scheduling program contained in a totally shared memory is operated upon by each computer as needed to determine work assignments. The scheduling function, is implemented in the program rather than in specialized hardware, thus avoids waste in computing power.



The programmer need not schedule; rather, he specifies brief sets of rules by which scheduling may be accomplished. Each computer module schedules itself, spontaneously establishing temporary master/slave ralationships with other computers for parallel operations. Simple or complex configurations are handled with equal ease. No major elements must perform critical functions. Those functions which are vital to system operation are simple or passive and can be easily and inexpensively duplexed to provide absolute system protection. Because of these unique features:

- All system elements may be in maximum use all of the time
- All modules communicate freely, without buffering or computational delays
- System balance is maintained automatically in all workload configurations
- No major system element is specialized to perform a single function
- A single failure cannot disable the entire system
- The program load is broadly flexible in real time
- Programming is straighforward and convenient



- Programs prepared independently may be processed simultaneously
- The system is readily expanded, in the field, with additional modules
- Processing rate can be increased by expanding the computer complement
- System balance and flexibility are maintained throughout expansion
- System expands to maximum complement without reprogramming.

SYSTEM ORGANIZATION

The Burroughs D825 Modular Processor is organized for a specific application in an appropriate complement of Computer Modules, Memory Modules, Input/Output (I/O) Control Modules, and a common exchange of I/O devices. Physically, a complete system, including power supplies, is housed in a number of standard cabinets, an operating console, various input/output equipments, and off-line circuit test equipment.

D825 organization is based upon the automatic operating and scheduling program (AOSP), a master program stored in totally shared memory. The AOSP is operated upon by each computer as needed to determine work assignments, and lies dormant until activated. Each computer schedules itself, establishing master/slave relationships with other computers for optimum handling of parallel operations. Hardware failure simply reduces the on-line equipment configuration, permitting normal operation to continue at a reduced rate. (Even the centralized elements, such as the common clock, the switching interlock, the automatic I/O exchange, and the AOSP are protectable for real-time environments which demand extraordinary reliability, by duplication of these simple but vital elements.)

The switching interlock is the focus of data flow within the system, providing automatic parallel routing and control of

intermodule communications and interrupt signals. The interlock resolves communication conflicts by scheduling rather than by buffering, accomplishing its function with a comparatively small amount of circuitry and without delay either for the no-conflict case or for the priority case of conflicting messages.

The Computer Module processes data and performs arithmetic operations in a synchronous serial-parallel manner at 3 megacycles. A thin-film register storage and operand stack in each Computer Module operates at the clock rate and greatly reduces the required accesses to Memory Modules. The command structure of the computer includes binary and alphanumeric instructions. Binary arithmetic may be fixed- or floating-point with the computer organization oriented toward efficient floating-point computation. The addressing structure of the computer has been designed to incorporate all of the power of a three-address machine. (Less than the maximum of three addresses can be processed with each instruction, with commensurate savings in instruction time and program storage.) Instructions are specified by use of strings of 12-bit syllables. An operation may consist either of a single operation syllable or of a number of complex syllable strings. Four instruction syllables are stored in each memory location for maximum program packing efficiency, but instruction strings need not conform to normal word boundaries.

Two types of storage are available for the Memory Module. One is a linear-select (word-organized), random-access, ferrite-core storage normally available only in computers designed for extreme environments. The other is Burroughs Fluxlok storage, functionally similar except that reading is nondestructive of the information stored. Fluxlok is unique among random-access nondestructive-read techniques in that it permits electrical alteration of data and employs standard ferrite cores. An important Fluxlok characteristic—vital to many military applications—is the complete protection afforded program and constants data against transient alteration. Memory Modules of either or both of these storage types may be used in a single D825 system.

I/O Control Modules, also housed two per standard module cabinet, consist essentially of control and data manipulation registers and associated decoding and timing circuits. Each controls, one at a time, any device of the I/O complement. The I/O exchange automatically connects control modules with specified I/O devices, on command from computer modules. The operating console, effectively an I/O device, displays system status to the operator, and permits him to effect inquiries and manual interrupts.

The D825 can be organized—and rapidly and simply expanded by appropriate addition of modules, in the field—in any combination of:

- 1 to 4 Computer Modules, each with clock-rate thin-film storage
- 1 to16 4096-word, high-speed, random-access, Memory Modules, either linear-select or non-destructively read Fluxlok
- Single or duplexed switching interlock, providing unbuffered module intercommunication
- 1 to 10 I/O Control Modules, each controlling any of the I/O devices
- 1 or 2 automatic I/O exchanges, connecting any I/O Control Module with any I/O device
- 1 to 64 I/O devices, in any combination, selected basically from: operating consoles, magnetic tape transports, magnetic drums, magnetic disc files, card punches and readers, paper tape perforators and readers, supervisory printers, high-speed page printers, selected data converters, real-time clocks, and intersystem data links.

Addition of switching interlock circuit cards effects the necessary changes to accommodate additional functional modules. In addition, the D825 can be multiplexed to form command and control systems of extreme size.

Speed

D825 clock rate is 3 megacycles per second. Execution times include fixed-point add of 2.33 microseconds and floating-point add of 6 microseconds. Thin-film registers and operand stack operate at clock rate. Memory rates include access time of 1 microsecond and read/write cycle of 4 microseconds. Random addressing and transferring of a full word to or from Memory Module is accomplished in 4 microseconds, establishing a data transfer rate of 250,000 48-bit words or 2,000,000 alphanumeric characters per bus per second. Module intercommunication, including input/output, flows without computer delay.

Capacity

One to four Computer Modules process 48-bit words (8 alphanumeric characters) in serial-parallel mode in fixed-point or floating-point. One to 16 simultaneously addressable, random-access, Memory Modules (optionally, rugged linear-select or electrically alterable nondestructive-read Fluxlok) store 4096 to 65,536 48-bit plus parity words. Thin-film storage holds 51 working registers, from 4 to 48 bits each. One to ten I/O Control Modules per bus can be operated simultaneously, each handling any of the maximum I/O complement of 64 devices.

Economy

D825 achieves economy of program storage space through use of variable-length syllable-string instructions; equipment economy through highly efficient circuits in a balanced serial-parallel configuration; and economy of computation time through automatic assignment of program segments, overlapped fetching of computer instructions and input/output transfers which are independent of, and simultaneous with, computation.

Reliability

D825 operates with total modularity and active spares. Since no single element performs a unique function, no single

failure can disable entire system. MTBF (mean time between failures) of Computer Module is 180 hours, and MTBF of all other system elements greatly exceeds this figure. Typical maximum system is totally available 95 per cent of the time, and 75 per cent of system is always available. System design includes self-diagnosis, automatic failure bypass, and automatic nonvolatile storage of register contents during power source over/under voltage conditions.

SYSTEM OPERATION

The D825 adapts instantly to real-time influence: to new programs, to changes in program priorities, and to manual or automatic interrupt signals. Its operational structure permits broad programming flexibility and efficient operation and program storage. Man/machine communication is comprehensive.

Parallel Operations

Each D825 Computer Module has exclusive use of a data transfer bus by which it can communicate, via the switching interlock, with any memory module, any I/O Control Module, or any other Computer Module in the system. The I/O Control Modules, share one or two busses.

Memory may be used concurrently by all Computer and I/O Control Modules. If two or more functional (computer or I/O control) modules simultaneously address the same Memory Module, the switching interlock automatically resolves the conflict, using a priority technique, and queues the lower priority items. One functional module gains immediate access while the other is delayed only until completion of the first memory transfer.

The rationale used to assign computers and other system modules to program segments is analogous to the assignment of weapons to targets in the point defense of a city against a complex airborne attack. The development of the basic AOSP philosophy stems, in fact, from studies conducted by Burroughs for the U. S. Army Signal Corps on the problem of point defense. In a manner similar to the assignment of

weapons, which is governed by weighting various criteria—maximize number of targets killed, minimize target penetration, or minimize damage done by enemy—the AOSP uses various criteria in forming the rules of assignment. For example, minimizing idle time of computers is essentially equivalent to completing all programs in minimum time. Alternatively, minimizing the running time of certain high-priority programs may be used as a criterion at the expense of delaying other programs.

Operator Access

The operating console in the D825 system is treated as an inquiry station and is coupled to the system as an I/O device. Inquiries from the console are handled by the interrupt procedures inherent in the design. Hence, the operator has access to the status of any operation, even in the full system, and is able to test and alter the schedule of events. Automatic monitoring of events can also be established, using the supervisory printer for reports to the operator. Console controls and indicators are therefore held to a bare minimum, although an input keyboard is supplied.

Operational Structure

The D825 is a 3-megacycle, synchronous, digital computing and data-processing system. Arithmetic processes and data flow within the system are serial-parallel in nature.

The D825 has been designed with a data word of sufficient length (49 bits including sign and parity) for almost all computing problems, and for really useful binary floating-point computation (36 bits of mantissa, including sign, and 12 bits of characteristic or exponent). This provides as much resolution for floating-point arithmetic as many large-scale computing systems offer in fixed-point arithmetic. In the alphanumeric mode, the D825 data word contains eight characters.

The order structure of the computer imparts unique flexibility and efficiency to programming through the use of variable-length instructions. Each instruction consists of

a string of 12-bit syllables. Instruction syllables are stored in memory, four syllables in a single word location. Instructions need not, however, conform to normal word boundaries, but may overlap; a five-syllable instruction, for example, may be stored as two syllables in the last half of one word location and three syllables at the beginning of the next, thus allowing efficient storage of variable-length instructions.

Operands called from memory to be operated upon are placed in a four-position stack of operand registers within the thin-film storage of the computer. The results of operations can be stored in memory or left in the operand stack for subsequent processing at the will of the programmer. The use of this temporary storage allows arithmetic operations to be performed much faster by automatically retaining selected temporary results within the computer.

The operand stack is a device, extremely useful in arithmetic computations, which reduces the number of references to main memory by holding partial or intermediate results of computation. The stack operates in two modes: normal and hold. In the normal mode, operation is analogous to the familiar plate stacks in cafeterias; when a plate is removed, the stack of following plates is moved up. In the hold mode, the top level of the stack is held, preventing upward movement of the rest of the stack. This condition prevails either until something is stored in the stack (moving it down) or until the operation is executed. The hold mode is a powerful device for list manipulation and can be used for squaring numbers.

The first syllable of an instruction supplies the operation code, and indicates, when applicable, whether the operands are in the operand stack or are to be fetched from memory, and whether the result is to be stored in memory or is to remain in the operand stack. Address syllables or syllable strings follow the operation syllable when memory accesses are called for. Each address syllable contains an eleven-bit literal address and an indirect address bit. The literal address may be added to the 16-bit base address register in order to refer to an area of memory known as the direct

address area. The contents of the direct address area location may be either an operand or another memory address. Indirect addressing of any desired number of levels is available by this technique.

Any of the three operand addresses which can be developed for each instruction may be modified by one of fifteen thin-film index registers. This capability, combined with the powerful indirect addressing capability of this system, provides immensely flexible subroutine control.

Automatic Interrupt Capability

To provide an additional mode of control, and to facilitate recognition and diagnosis of failures, an automatic interrupt system is included as an integral feature of the D825.

All interrupts arising in a D825 System are recorded in the central interrupt register. Each Computer Module has continuous access to the interrupt register through individual mask registers. The mask register in each computer is set by the AOSP to indicate which interrupts each computer will process. When a Computer Module senses a one output from its mask register, it immediately processes the appropriate interrupt.

Two advantages result from the fact that the mask registers are controlled by the AOSP:

- The AOSP can dynamically allocate the processing of specific interrupt conditions to any of the Computer Modules
- The AOSP can establish a master/slave relationship between any two computers by masking out slave-to-master interrupts.

When an interrupt is received from another Computer Module, the interrupted computer branches to the location specified by the interrupting computer. For all other interrupts, the computer branches to the AOSP to determine the interrupt cause and the course of action to be taken.

Typical interrupt conditions are related either to aspects of control:

- Arrival of an urgent I/O request
- Completion of a specified I/O operation
- Inquiry initiated by operator at console
- Arithmetic overflow
- Running down of elapsed time clock

or to malfunctions of the system:

- I/O malfunction (broken tape, card jam, parity errors)
- Illegal address or instruction, or parity error
- Equipment failure occurring in a major system element
- Power source failure.

As indicated, each Computer Module may establish a master/slave relationship with any other Computer Module in the system, when operation of the AOSP indicates a program branch suitable for parallel processing. The master Computer Module transmits to another Computer Module (or modules) the base address (or addresses) of the program segment (or segments) to be run. The interrupted slave computer module automatically stores its stack and instruction register contents, executes the designated program segment, then returns to its previous program segment.

SECTION III

DETAILS OF THE D825

The D825 is unique in its orientation toward military related applications. The design utilizes advanced circuit and packaging techniques developed and proved by Burroughs in military computing systems for ground-based, mobile, airborne, and shipborne applications. This section presents the details of D825 design and performance; general electrical and mechanical characteristics; detail specifications of the major D825 modules; and lastly details of D825 programming.

ELECTRICAL AND MECHANICAL DESIGN

All electrical and mechanical design techniques used in the D825 are of known stable and reliable performance. The following paragraphs present the details of the logic circuitry, thin film registers, memories, input-output drive capabilities, and mechanical design.

Logic Circuitry

The logic circuitry on the D825 System employs Burroughs proprietary Hybrid Transistor-Diode Logic (HTDL) technique. This circuitry has been proved over a wide variety of severe military applications which include the 1.3 megacycle Airborne Bombing and Navigation Computer, a 10-megacycle large-scale data processing system, and an airborne data processor. HTDL offers the following advantages:

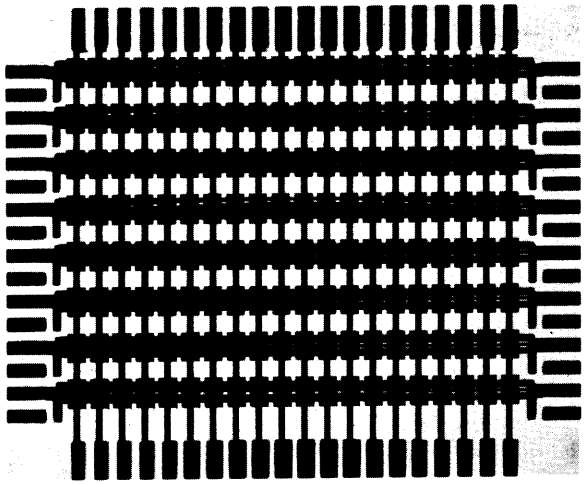
- Optimum use of transistor gain-bandwidth product.
- Noncritical transistor parameters

- Large fan-in and fan-out capability
- Maximum system reliability through minimum number of circuit components
- Minimum component cost through use of inexpensive diode gates and use of transistors in dual function as amplifying gates.

Because the HTDL technique does not impose rigid specifications on the transistor or on any of the circuit components, it is both economical and reliable. These advantages have been verified by extensive production and field experience.

Thin-Film Memory

The 80-word, 18-bit, magnetic thin-film memory which serves as storage registers within the Computer Modules is a word-organized array. The read/write cycle for the thin-film memory is 0.33 microseconds.



The thin-film memory for the D825 Computer Module is constructed in eight planes of 200 bits each. These planes have bits of nickel-iron alloy vacuum-deposited on glass substrate. Preferred magnetic orientation of the bits is established by deposition under the influence of a magnetic field. Uniformity of electrical characteristics is obtained by extremely precise control of the deposition process.

The magnetic characteristics exhibited by the films are an almost perfectly square hysteresis loop in the preferred direction and almost perfect B-H proportionality at right angles to this direction.

In operation, a drive field is applied in the proportional direction, with switching taking place on the rise of drive current. The drive pulse brings the films to a demagnetized state, producing output pulses which are, for a ONE or for a ZERO, of the same shape but of opposite polarity. The sense line links the film at right angles to the drive line, and therefore sees a square-loop device. Before the word drive falls to zero, current is turned on in an information drive line parallel to the sense line, and the polarity of this current controls which of the two states the film will take when the drive current releases the film spot.

Storage Memories

The 4096-word main memory modules are linear-select (word-organized) ferrite-core arrays which operate conservatively with a cycle time of 4.0 microseconds.

In military applications, the linear-select memory technique is vastly superior to the widely used coincident-current memory system as it offers the capability of high-speed operation while allowing looser circuit tolerances and a much greater temperature range. Burroughs extensive experience with memory technique includes the first operational memory of this type in the NADAC airborne computer, extensive production experience with SAGE, and use in the Polaris Stabilization Data Computer.

Input-Output Drive Capability

The following information is submitted to assist in the evaluation of the Modular Processor with respect to special input-output devices. The I/O Control Module is capable of driving, without the use of special drivers, coaxial lines with an impedance of 93 ohms or higher and of a length not exceeding 200 feet.

Maximum data transfer rate of the D825 system is limited by memory-bus characteristics to 250,000 computer words per second or over 12 million information bits per second. Thus, a single I/O Control Module has the capability of controlling one peripheral input-output equipment at a time with a limiting data rate of 12×10^6 bits per second. Since few input-output equipments are capable of this rate, additional I/O Control Modules can help utilize this maximum data rate by permitting simultaneous operation of input-output equipments. In addition, added I/O Control Modules permit simultaneous input of raw data and output of processed data.

Mechanical Design

The Modular Processor equipment cabinet is a multi-purpose cabinet and is used to house all of the system elements with the exception of some of the peripheral devices. Each of these multi-purpose cabinets includes a standard unitized power supply which is sufficient to provide regulated power for the equipment it contains.

A single Modular Processor equipment cabinet houses any of the following:

- A Computer Module D825-1
- 2 Memory Modules D825-2
- 2 I/O Control Modules D825-4 with additional space and power available for special-purpose input-output devices

- A Magnetic Tape Module D825-40
- A Paper Tape Module (reader and punch) D825-43
- 2 Magnetic Drum Modules D825-47

Circuitry within each of the major system modules employs standard printed circuit cards and subassemblies. The printed circuit cards and associated fabrication techniques are identical with those employed for military equipments presently in production. The use of the country's most completely automated electronic computer production facility (Burroughs Military Electronic Computer Division) - in which drilling, plating, component insertion, dip soldering, and card test are automatically performed - assures maximum economy with high uniformity and reliability. The Modular Processor equipment is of welded steel frame construction with integral adjustable leveling pads, with provision for either surface or subsurface interconnection cables. Swing-out racks carry the printed circuit cards to provide ready accessibility for maintenance and at the same time assure minimum space requirements. The unitized power supply, designed to provide for the needs of any of the module types, is mounted at the top of each basic cabinet. Floor loading does not exceed 200 lb/sq feet.

The basic modular cabinets are designed so that room air circulation provides cooling. Input air is drawn in at the bottom and exhausted at the top of each cabinet.

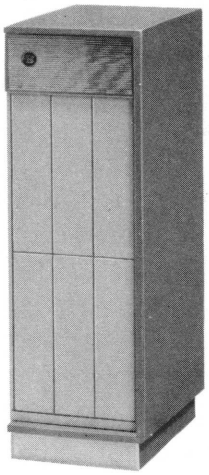
MAJOR D825 MODULES

The major D825 Modular Processor modules discussed are as follows:

D825-1	Computer Module
D825-2	Memory Module
D825-3	Switching Interlock
D825-4	Input-Output Control Module
D825-40	Magnetic Tape Module
D825-41	Card Punch Module
D825-42	Card Reader Module
D825-43	Paper Tape Module
D825-44	Electrographic Printer Module
D825-46	High Speed Printer Module
D825-47	Magnetic Drum Module
D825-48	Magnetic Disc File Module

COMPUTER MODULES D825-1

The system can accommodate up to four Computer Modules. Each Computer Module consists of three functional areas. The arithmetic unit is made up of 3 registers with associated control. The second area is a set of approximately 50 registers contained in a small thin-film magnetic storage. The third area is the control which includes capability for indexing, address accumulation and indirect addressing; and the command and subcommand matrices. The central buffer (also included) serves as the routing source for these various units. All circuitry operates at a 3-megacycle clock rate.



The central buffer register is a multi-purpose register. To initiate a memory transfer, the memory address is transferred to the central buffer register. The portion of this address used to designate a Memory Module is sent as dc levels to the switching interlock circuitry of the memory trunk. Address data for the Memory Module and information words entering the Computer Module from the memory module are transmitted through the central buffer register at least six bits at a time.

The A register, B register, and C register are the working arithmetic registers of the computer module. The A and B registers with associated complement and adder circuitry perform the actual arithmetic operations. For floating-point (12-bit signed exponent and 36-bit signed mantissa)

and fixed-point operations, the A, B and C registers are used as shift registers. The A register is capable of shifting 12, 6 or 1 places to the right or 1 place to the left.

The index control register is used as temporary storage for address arithmetic.

The command register is a 12-bit register that holds the operation syllable being executed and provides the dc levels for driving the command and subcommand matrices.

The MD counter controls the number of add or subtract cycles to be executed during multiply or divide operations. The counter also controls the number of shifts to be executed during an instruction.

The Computer Module utilizes thin-film storage for:

- 7 operand registers,
- 2 program storage registers,
- Program counter,
- Base address register,
- Base program address register,
- 15 index registers,
- 15 index comparison limit registers,
- Index address register,
- Real time clock, and
- Interrupt system registers.

The seven operand registers include four operand storage registers which make up the thin-film operand stack; the TFC register whish is used to store the least significant half of a double-length product, the quotient during division, and the remainder when division has been completed; and the full word masks used in the mask and merge instruction.

The two program-storage registers provide storage for eight instruction syllables and permit overlapped instruction fetch.

The base address register holds the address of the starting location of the data direct-address area.

The base program register holds the starting location of the program address area.

There are 15 index registers, and 15 comparison limit registers. Any three of the index registers may be addressed by each index address syllable and used to modify each operand address. The index registers may be incremented, decremented, and compared; the arithmetic unit is utilized for this operation.

The thin film index address register is a 12-bit register that is used to hold the addresses of the three index registers currently being used. This register is loaded directly from the program registers with the syllable immediately following the address syllable upon which indexing is to be performed.

The contents of the real-time clock, a 24-bit register, is automatically read out and decremented once every 10 milliseconds. The real-time clock may be sampled by the program or, through use of a control flip-flop, can be counted down and used to initiate an interrupt when the count reads a zero.

The interrupt system registers provide storage for data in the operational registers in the event of an interrupt.

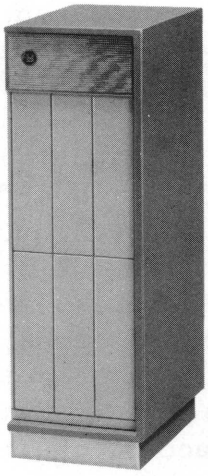
In the interrupt system there is an over-under voltage detector which will detect and signal excursions of primary power beyond fixed voltage limits. The out-of-tolerance signal, which has a maximum delay of 10 microseconds, sets an interrupt condition and causes the computer module to store sufficient information to restart the program without loss of data. Provision is made for automatic program restart by automatically reloading the stored data back into the flip-flop registers. The power supplies themselves have a sufficiently long time constant that this scheme protects the hardware, program, and data from all primary power transients and failures, and allows continuation of the program as soon as stable primary power is restored.

The interrupt system also handles interrupts arising from such conditions as arithmetic overflow, running down of the real-time clock, illegal orders, parity errors, special input-output requests and situations, etc. All interrupts are recorded in a central interrupt register. Each computer module has access to this interrupt register through its own interrupt mask register. When a particular condition has set a "one" at some bit position in the interrupt register, and when the program accessible mask register is set to recognize the condition, a program interrupt occurs. This interrupt stops the program being executed, stores sufficient registers to allow continuation of the interrupted program at a later time, and transfers control to a program to service the interrupt.

MEMORY MODULES D825-2

The system accommodates up to 16 Memory Modules (two per cabinet). Each Memory Module contains a random-access, linear-select, ferrite-core memory of 4096 words. Each word contains 48 information bits and one parity bit. The modules also contain independent read, write, and regenerate circuitry as well as necessary addressing circuitry. A complete read-write cycle requires less than 4 microseconds. Read requests are made to a particular Memory Module by transmitting two six-bit characters to the module

to designate the address of the desired word. Less than one microsecond after the completion of this transmission, the desired word is in the module's data register, and word regeneration and transmission of the word to the requesting module then begins in parallel. The complete cycle from commencement of the transmission of the word address to a state where data word regeneration and transmission is complete and the module is ready to accept another word address, requires four microseconds. Likewise, the complete cycle for writing new information into memory including the transmission to memory of both the word address and the data also requires four microseconds.



There are up to five trunks in the system capable of exchanging information with the Memory Modules. Three of these trunks are connectable to Computer Modules, one Computer Module per trunk. The fourth trunk is connectable either to a fourth Computer Module or else to a number of Input-Output Control Modules where this number may be between one and ten. The fifth trunk is connectable to a similar number of Input-Output Control Modules.

Any module terminating one of these trunks is capable of exchanging information with any Memory Module. Provided that each trunk is exchanging information with a different memory module, all five trunks can simultaneously exchange information with memory at a rate of one 48-bit word per trunk per four microseconds. In the event that two or more trunks (or the devices terminating them) wish to be connected

to the same Memory Module, the conflict is resolved by a priority scheme with the highest priority request being immediately granted and the lower priority requests being held in abeyance and being serviced immediately on completion of the higher priority request. In the event of the simultaneous occurrence of a number of conflicts, conflict resolution is performed in parallel with no lost time to any of the Memory Modules involved in the conflicts.

SWITCHING INTERLOCK D825-3

The switching interlock interconnects the various modules in the system. The switching interlock is divided into two functional sections: the bus allocator which provides protection against time conflicts, and the cross-point switch which effects the actual switching.

The bus allocator defines and resolves all time conflicts resulting from simultaneous requests for the same bus or module. Conflicts are resolved by having the conflicting requestors queue up according to a priority transmitted with each request. The priority system is pre-emptive in that a new request with a high priority will precede a low-priority request already in the queue.

The bus allocator consists of five subsections: conflict detector matrix, priority matrix, address availability matrix, queue matrix, and command matrix. The conflict detector matrix and priority matrix respectively provide conflict priority information to the queue matrix so that requests are placed in their proper order in the queues. Requests found not to be in conflict with others are put in queues of zero length; that is, they are serviced immediately. The conflict detector matrix detects conflict by comparing each of the six possible requests with the other five module requests. A conflict matrix is generated showing which busses are in conflict.

The priority matrix decodes priority bits transmitted with each memory access request and generates a priority matrix. The outputs of the conflict matrix and the priority matrix are logically ANDed together and set storage flip-flops of the queue matrix.

The queue matrix consists of flip-flops arranged in a 5 X 5 matrix. Sampling signals are propagated vertically through the matrix, appearing at the output only when all the flip-flops in the column are in the reset state. Output pulses, in addition to activating the command matrix, are used to reset all the flip-flops in the corresponding row; that is, the output pulse from column 4 resets all the flip-flops in row 4.

The address availability matrix determines if any of the requests are for busy addresses, and generates signals which inhibit the output of the command matrix when a busy address is requested.

The command matrix accepts inputs from the queue matrix and generates switching commands for the cross-point switch unless inhibited by the address availability matrix.

INPUT-OUTPUT CONTROL MODULES D825-4

The system can accommodate up to ten I/O Control Modules per memory trunk allocated to IO. The I/O Control Modules are capable of controlling up to 64 external devices. The execution of a "Transmit to I/O" order by a computer module causes the transmission of a 48-bit I/O descriptor to any non-busy I/O Control Module (causing a branch in the computer program if none are available). The instructed Control Module then decodes its descriptor and acts accordingly. Various fields in the descriptor have the following interpretations:

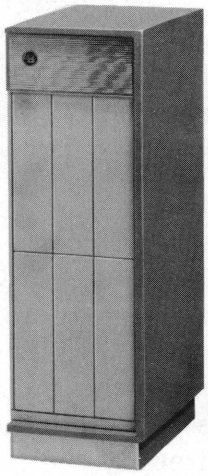
Field 1 - The IO device to be connected by the I/O Control Module,

Field 2 - The memory location to be involved in the first memory exchange,

Field 3 - The number of successive memory locations to be used,

Field 4 - Bits which may be decoded by the external device and used for its control, and

Field 5 - Additional internal status and interrupt bits as necessary for efficient operation.



The registers of the I/O Control Module include a full-word register for transmission and reception of data to and from memory, a register for the packing and unpacking of data, and sufficient control circuitry for the registration and utilization of the control word. When an I/O Control Module is connected to an output device, it requests, over its memory trunk, the contents of the memory location indicated by field 2 of its descriptor. When this information has been received in its transfer register, and gated to the unpacking register, field 2 is stepped up, and field 3 is stepped down. The first six bits in the unpacking register have parity added (when applicable) and are transmitted to the selected output device. When this device has sent a strobe indicating readiness to accept another character, it is transmitted until the full computer word has been transferred, at which time the whole cycle is repeated. When field 3 reaches zero the block transfer is complete and is terminated, and the I/O Control Module makes indication of this fact to the system under the direction of field 5. When an I/O Control Module is connected to an input device, it strobes this device to indicate readiness to accept a character. It then awaits a strobe from the input device indicating that the voltages on the input wires are to be interpreted as a character. This cycle is repeated until eight characters have filled the packing register, at which time the packing register is gated into the

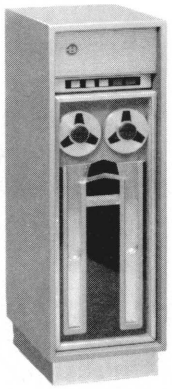
transfer register. The word now in the transfer register is transmitted to the memory location designated by field 2 of the descriptor. Field 2 is stepped up and field 3 is stepped down. As soon as the packing register has been gated into the transfer register, the input device is strobed for the continuation of the information transfer. When field 3 reaches zero, the process is terminated and the I/O Control Module indicates this fact to the system under the direction of field 5.

The communication between an I/O Control Module and external devices proceeds at a rate controlled by the external device which rate may reach 1/3 μs per 6-bit character, for devices sufficiently close to the module, until the full word is assembled. The rate at which words may be exchanged with memory is not limited by the nature of the I/O Control Module. In the case where only one I/O Control Module is accessing memory and no other device is requesting access to that Memory Module, the maximum rate is one 48-bit word every 4 μs.

Each I/O Control Module requests service over the I/O Memory trunk for only the actual time (4 microseconds) required to transmit a memory address and a data word. Circuitry resolves conflicts between different I/O Control Module requesting the same trunk in a manner analogous to the case of different trunks requesting the same memory module. This conflict resolution is essentially zero-time in the sense that the trunk is capable of an 12-megacycle data word bit rate even when communicating with a number of I/O Control Modules.

MAGNETIC TAPE MODULE D825-40

The D825-40 magnetic tape system operates independently of the processor. Reading, writing, backspacing, rewinding, and erasing operations are under system control.



The D825-40 Magnetic Tape Module accepts data in either binary or single-frame alphanumeric form. Tape format is compatible with IBM Model 729-II and 729-IV magnetic tape units. Standard tape one-half inch in width is used. Tapes are mounted on reels which contain up to 3600 feet of tape and have a maximum diameter of 10 1/2 inches.

Data may be stored in two densities, either 200 or 555.5 frames per inch. One frame contains either six binary bits or one six-bit alphanumeric character. Tape speed is 120 inches per second, a transfer rate of 24,000 characters per second for a density of 200 frames per inch, and 66,660 characters per second for a density of 555.5 frames per inch. Packing density is selected by a switch on the unit.

Tape is rewound at a speed of 340 inches per second. Start or stop time is 5 ms. The dual-gap read-write head of the D825-40 Magnetic Tape Module provides automatic checking of write operations.

The tape unit operates in two modes: local or remote. Local manual control of the unit is provided by a Local-Remote switch on the operator's panel. An indicator denotes which operating mode is in effect.

Mounting and removal of tape reels is facilitated by quick-action reel locks. A Reel Brake Release switch permits loading or unloading of the tape. A write ring must be installed on a reel to permit writing or erasing, thus preventing accidental destruction of files. After the tape reel has been mounted on the unit, activating the Load switch causes the tape to be drawn into the slack loop mechanism, and to be automatically positioned at the beginning-of-tape marker, ready for operation. An Unload switch is used to reverse the load procedure for removal of the tape reel. The unit must be in local mode for these operations.

A Ready indicator shows when the transport is in a ready state. A Write Warning light is turned on if the reel installed on the transport is equipped with a write ring.

Tape format consists of seven recorded channels across the tape. The information tracks represent either single-frame alphanumeric or binary information and a track provides a parity check for each frame. The non-return-to-zero method is used for recording.

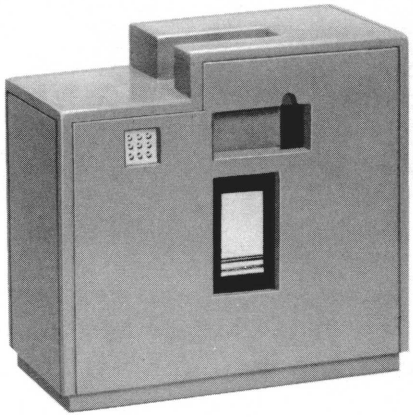
Reading and writing can be done in either binary or alphanumeric mode, providing complete code flexibility to the system. The alphanumeric mode carries an even parity. That is, a parity bit is recorded simultaneously with each character if an odd number of bits represents that character in the information channels. The binary mode carries an odd parity. A parity bit is recorded if there is an even number of bits in the information frame.

It is possible to write interspersed binary and alphanumeric records in the binary mode.

A longitudinal check character is written after the last character of each record. This consists of a parity bit, automatically recorded in each track with an odd total bit count. These parity bits maintain an even number of one-bits in each track for the entire record length, regardless of the code used.

CARD PUNCH MODULE D825-41

The card punch will feed, punch, check, and stack 80-column cards in both standard and postcard thicknesses at a maximum rate of 100 cards per minute. Functional controls are located on a plugboard and on the operator's control panel.



Double-punch and blank-column detection units are available in groups of 20 as optional devices. The punch contains a single-panel plugboard for the wiring of double-punch and blank-column checking. The hopper and stacker can hold 800 cards each.

CARD READER MODULE D825-42

This 800 cpm reader can read cards of 51, 60, 66, or 80 columns. A card file, however, must be consistent in column length and card thickness. The information is read serially, column by column. Card data may be represented in standard tabulating card code or straight binary code. Each card file must contain cards prepared in only one code.

Invalid characters are sensed and replaced by six zero bits and an error indication is supplied to the computer. Binary codes are read column by column, six bits at a time. Since there are 12 bits in a binary column, each card column occupies the equivalent of two six-bit characters.

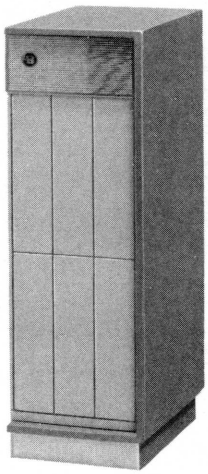
The read circuitry is monitored during each card cycle, and when an error is detected an indicator is turned on. The operator may signal an end-of-file condition by depressing the Card Reader End-of-File key, when the card hopper is emptied. The reader may then run out the two or three cards still inside the reading mechanism and provide an end-of-file signal to the Input/Output Channel.

The hopper and stacker of the card reader have a capacity of 2400 cards each, and allow removing or adding cards while the reader is operating.

PAPER TAPE MODULE D825-43

The paper tape reader has the capability of reading standard seven-hole punched paper tape at speeds up to 1000 characters per second while maintaining the capability of stopping on a single character. It is able to detect two special tape characters, and instead of transmitting these over its character lines, two special wires are pulsed for informing the

I/O Control Module to terminate packing and terminate input at the end of words and records respectively. A character request from the I/O Control Module starts motion of the tape reader, and this motion continues until either an end of record character is encountered or until the character request strobe ends.



The paper tape punch has the capability of punching standard seven-hole paper tape at up to 100 characters per second.

ELECTROSTATIC PRINTER MODULE D825-44

In the electrostatic printer, the print heads deposit electrostatic charges on the surface of coated paper in the form of the character to be printed. The image is developed with powdered ink which adheres to the charged areas, and the ink is fixed by a heated roller. Since this type of printing operation involves very few moving parts, operation is highly reliable and very little maintenance is required.

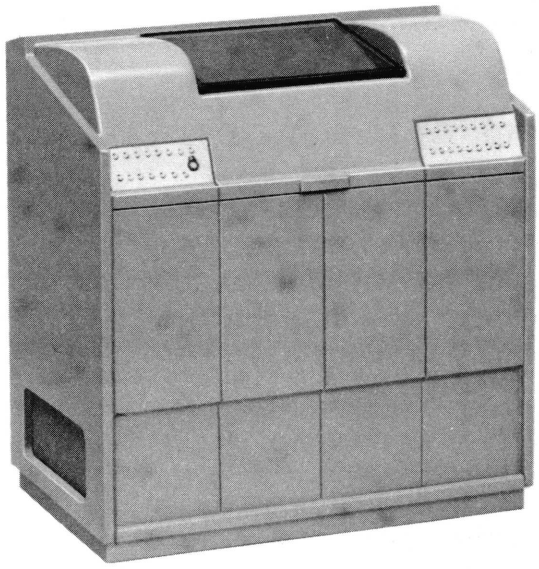
The printer prints over six 72-character lines per second or 360 lines per minute. It accepts six bit parallel characters at rates up to 500 per second. A high speed electronic column switch determines the sequential operation of 72 print heads so that printing occurs serially across the page. A column counter is reset to zero by the carriage return character, and a line feed character advances the

paper. Under continuous operation, a line of printing is visible two seconds after recording.

HIGH SPEED PRINTER MODULE D825-46

The printer operates at 650 lines per minute. There are 120 print positions per line, and 63 characters plus a blank are available for each print position. Two optional character sets are available to provide complete flexibility for all printing requirements. There are 10 characters per inch horizontally, and either six or eight lines per inch vertically.

The printer accepts 15 words of alphanumeric information for each line of print. This information is transferred from ascending memory locations a character at a time and accumulates in the 120-position buffer of the printer. When the buffer is completely loaded, the line is printed. Access to a print cycle is immediate.



Continuous paper forms are used. They may be from 5 to 20 inches wide, including margins, and a form may have a maximum length of 22 inches. Form adjustments require no special tools and drum clearance may be adjusted. Each tractor mechanism which controls horizontal placement of the form can be adjusted independently when the machine is stopped. Once installed, the form can be shifted left or right in minute increments while the machine is operating. Precise vertical form adjustments can be made in either direction when the printer is stopped. Processed forms are stacked.

Legible printing can be produced on forms from .0025 to .020 inches thick. Up to six-part forms on white sulfite bond can be printed, using .001-inch carbons. This number can be increased by using premium papers and carbons.

A vertical format punched tape, working in conjunction with the system, controls the vertical format of the printing, including such operations as skipping to a new page or skipping lines within a page.

The printer produces an end-of-page signal, a print-check signal, and a not-ready signal.

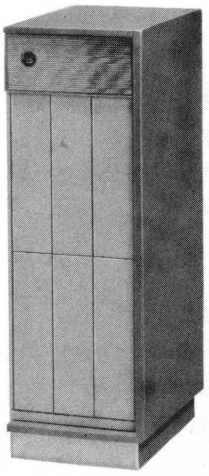
Print checking consists of a parity check when characters are read into or out of the print buffer. Drum synchronization

is checked by means of the drum position counter to assure that the drum position and timing circuits agree.

MAGNETIC DRUM MODULE D825-47

The storage drum is a high-speed mass storage device providing rapid access to program segments, subroutines, and large blocks of data in addition to those which can be held in core memory. It communicates with Memory Modules through an Input-Output Control Module.

The drum is organized in 64 six-channel information bands, each band containing 512 words. Total storage capacity is 32,768 words. The drum rotates at a rate of 3600 rpm, and has a read-write speed of 8.1 microseconds per character. Average access time to a word on the drum is 8.5 milliseconds or 18.5 milliseconds if switching bands. Information can be retained on the drum indefinitely without regeneration.



A longitudianl parity of six bits is recorded at the end of each 48-bit word. The transfer of information between the drum and an Input-Output Control Module is made character by character, while transfers between the control module and Memory Modules are by word. Each word on the drum is addressable. Reading or writing may start at any drum address.

MAGNETIC DISC FILE MODULE D825-48

The magnetic disc file is a mass storage module storing up to 3 million 48-bit words. It contains 16 31-inch two-sided discs with 64 air-supported heads. There are 256 tracks per surface, with a maximum bit density of 400 bits per inch. Average access time is 158 milliseconds, and the transfer rate is 251,320 bits per second from the inner zone and 502, 640 bits per second from the outer zone. It communicates with the Memory Modules through an Input-Output Control Module.

D825 MACHINE LANGUAGE PROGRAMMING

The program consists of strings of 12-bit syllables of three types: operation, address and index. The operation syllable consists of a command code and three address indicators. Each address indicator designates whether the operand should come from the operand stack or from a memory address defined by a following address syllable; whether or not the stack should be held; and whether or not the address syllable should be indexed. Address syllables are of several types including operand memory address, branch, number of shifts and other special syllables. Index syllables consist of three 4-bit addresses of index registers in the thin-film memory.

The three implied address indicators enable the following forms of instructions:

- stack, operation, stack - stack S_i OP $S_{i-1} \rightarrow S_i$
- stack, operation, stack - memory S_i OP $S_{i-1} \rightarrow m$
- stack, operation, memory - stack S_i OP $m \rightarrow S_i$
- stack, operation, memory - memory S OP $m \rightarrow m$
- memory, operation, stack - stack m OP $S_i \rightarrow S_i$
- memory, operation, stack - memory m OP $S_i \rightarrow m$
- memory, operation, memory - stack m OP $m \rightarrow S_i$
- memory, operation, memory - memory m OP $m \rightarrow m$

The operand stack is a device, useful in arithmetic computations, which reduces the number of references to main memory by holding partial or intermediate results of computation. The stack actually consists of four registers (S_1, S_2, S_3, S_4) and a bi-directional cyclic counter which determines which register is currently available. The stack operates in two modes: normal and hold. In the normal mode, the operand is fetched from the register currently selected by the counter and the counter is stepped after the fetch. For stores, the counter is first stepped in the opposite direction and the operand is then written into the newly selected register. In the hold mode, the counter is not stepped.

The address and index syllables can be combined to effect both direct and indirect addressing. Each operand address syllable contains one indirect address bit and eleven bits of literal address. For direct addressing, the literal address is added to the base address register. If the address indicator of the operand syllable calls for indexing, an index syllable follows the operand address syllable. The index syllable contains the addresses of three index registers. One, two or three of these registers may be added to the literal + base register to form the effective address. An index address of zero indicates no addition. The general form of the effective address is then literal + base address register + index register A + index register B + index register C.

N-level indirect addressing is provided as follows: If the indirect address bit of the operand address syllable is a one, the normal effective address is computed. The least significant part of this address is fetched from the memory. If the indirect address bit is a zero, the literal part becomes the effective address of the operand. If the indirect address bit is a one, the literal bits are added to the base address register and the contents of this address is fetched from memory. The process is repeated until a zero is found in the indirect address bit.

An estimate of the running time for a set of instructions on a single D825-1 computer module may be made by summing:

- 9 microseconds for every word of program (4 syllable) processed, plus

- 4 microseconds for every operand or indirect address fetched, plus
- 1 microsecond for every operand stack reference, plus
- 2 microseconds for every address which is indexed, plus the listed instruction execution time.

From this may be subtracted 5 microseconds for every word of the program whose fetch can be overlapped with the execution of the previous instruction. Operations which permit this overlap include binary multiply and divide and all floating point operations.

In the following description of the operations, the following abbreviations and symbology are used:

S_1	The first or top level of the stack
S_2, S_3, S_4	The lower positions of the stack
( )	The contents of
$\overline{(\ )}$	The ONEs complemented contents of
0_1	The first address
0_2, 0_3	The second and third addresses
.	Logical AND
V	Logical OR
Ⓥ	Logical EXCLUSIVE OR
$(\ )_{a-b}$	Register or word, bits a to b inclusive

The various classes of instruction are presented in the following paragraphs. Each instruction is followed by its execution time in microseconds, the three-letter mnemonic code of the operation syllable, and a symbolic and textual description of the operation.

Arithmetic and Logical Instructions

Floating Add 6.0 FAD $(0_1) + (0_2) \rightarrow 0_3$

Add the signed binary floating-point number in the location specified by 0_1 to the signed binary floating-point number specified by 0_2, and store the results in floating-point format in the location specified by 0_3.

Floating Subtract 6.0 FSU $(0_1) - (0_2) \rightarrow 0_3$

Same as FAD except that (0_2) is considered as having its sign reversed.

Floating Multiply 40.0 FMU $(0_1) \times (0_2) \rightarrow 0_3$

Same as FAD except that the operation is multiplication.

Floating Divide 70.0 FDV $(0_1) \div (0_2) \rightarrow 0_3$

Same as FAD except that the operation is divide.

Convert Binary to Floating Point 6.0 CBF 0_1 (Binary $\rightarrow 0_2$ Floating)

Interpret the contents of the location specified by 0_1 as a signed binary number. Convert this to normalized floating point format and store it in the location specified by 0_2.

Binary Add 2.33 BAD $(0_1) + (0_2) \rightarrow 0_3$

Same as FAD except that the operands and results are signed binary numbers and the arithmetic is straight binary.

Binary Subtract 2.33 BSU $(0_1) - (0_2) \rightarrow 0_3$

Same as BAD except that (0_2) is considered as having its sign reversed.

Binary Multiply 51.0 BMU $(0_1) \times (0_2) \rightarrow 0_3$

Same as BAD except that the operation is multiplication. The operands are signed binary fractions. The high order product is stored in 0_3 and the low order produce is stored in the thin-film C (TFC) register.

Binary Divide 95.0 BDV $(0_1) \div (0_2) \rightarrow 0_3$

Same as BAD except that the operation is division. The remainder is stored in the thin-film C (TEC) register.

Round 2.33 RND $0_1 \rightarrow 0_2$ (Rounded)

The contents of 0_1 are rounded if the most significant bit of the thin-film C (TFC) register is ONE.

Logical AND 2.33 LAN $(0_1) \cdot (0_2) \rightarrow 0_3$

The contents of the location specified by 0_1 are logically ANDed bit-by-bit with the contents of the location specified by 0_2 and the result is stored in the location specified by 0_3. The sign bits are also ANDed.

Logical OR 2.33 LOR (0_1) V $(0_2) \rightarrow 0_3$

Same as LAN except that the operation is OR.

Logical EXCLUSIVE OR 2.33 LXR (0_1) V $(0_2) \rightarrow 0_3$

Same as LAN except that the operation is EXCLUSIVE OR.

Logical COMPLEMENT 2.33 LCM $(\overline{0_1}) \rightarrow 0_2$

The ONEs complement of the contents of the location specified by 0_1 are stored in the location specified by 0_2.

Change Sign 2.33 CHS $(0_1) \rightarrow 0_2$

The sign of the contents of the location specified by 0_1 is reversed. The result is stored in the location specified by 0_2.

Set Sign plus 2.33 SSP $|0_1| \rightarrow 0_2$

The sign of the contents of 0_1 is set to plus and the result stored in 0_2.

Set sign minus 2.33 SSM $|0_1| \rightarrow 0_2$

The sign of the contents of 0_1 is set to minus and the result stored in 0_2.

Decision Instructions

Compare	3.0	CEQ, CGR, CLS

Compare the contents of the location specified by 0_1 algebraically with the contents of the location specified by 0_2 for the indicated condition (EQ = equality, GR = greater than, LS = less than). If the condition is true, take the next instruction from the address specified by adding 0_3 to the Base Program Register (BPR). Otherwise, continue in sequence.

Alphanumeric Compare	3.0	ACE, ACG, ACL

Same as CEQ, CGR, CLS except that the comparison is alphanumeric.

Branch on Bit	1.33	BRB

If the low order bit of the contents of the location specified by 0_1 is a ONE, take the next instruction from the address specified by adding 0_3 to the Base Program Register (BPR). Otherwise, continue in sequence. In either case, perform a 48-bit end-around right shift one position on (0_1). Store the result in 0_2.

NOTE: BRB is used for decision making and control. It allows the programmer to specify a preset but variable path through his program.

Branch on Condition	1.33	BRC

If the condition corresponding to a ONE in the program syllable(s) is true, take the next instruction from the address specified by adding 0_3 to the Base Program Register (BPR). Otherwise, continue in sequence.

Field-Defined Operations

Field-defined instructions permit the packing of several operands in one word, such as alphanumeric characters or small numeric values. The following instructions are field defined. Fields may vary in size and one to 48 bits and may start at any point in the word as long as the field does not

exceed the boundaries of the word. For arithmetic operations, the low-order bit of the field is interpreted as the sign.

Only the instructions listed below may be field defined. Except for the variable operand lengths, they are the same as the corresponding non-field instructions.

Binary Add, Field	BAF	$(0_1)_F + (0_2)_F \rightarrow 0_3, F$
Binary Subtract, Field	BSF	$(0_1)_F - (0_2)_F \rightarrow 0_3, F$
Binary Multiply, Field	BMF	$(0_1)_F \times (0_2)_F \rightarrow 0_3, F$
Binary Divide, Field	BDF	$(0_1)_F \div (0_2)_F \rightarrow 0_3, F$
Logical AND, Field	LAF	$(0_1)_F \cdot (0_2)_F \rightarrow 0_3, F$
Logical OR, Field	LOF	$(0_1)_F \vee (0_2)_F \rightarrow 0_3, F$
Logical EXCLUSIVE OR, Field	LXF	$(0_1)_F \veebar (0_2)_F \rightarrow 0_3, F$
Logical COMPLEMENT, Field	LCF	$(\overline{0_1})_F \rightarrow 0_2, F$
Compare, Field	CEF, CGF, CLF	
Alphanumeric Compare, Field	AEF, AGF, ALF	
Transmit, Field	TRF	$(0_1)_F \rightarrow 0_2, F$

Manipulation and Control Instructions

This class includes shifts, clears, loads, and stores. Shift instructions are for manipulating individual bits or characters of the operand in order to rearrange data or for isolating data to be operated on. End-around shifts and end-off shifts are provided. The latter drops bits off one end and introduces ZEROs on the other. Execution times for shifts are 2.67 μsec plus 0.33 μsec for each shift subcommand performed. Left shifts are of one bit or right shifts are of 1, 6, 12 bits.

Shift Designation	Shift Description							
	Left	Right	End-Around	End-Off	Arith.	Logical	Single	Double
0	1	0	1	0	1	0	1	0
1	0	1	1	0	1	0	1	0
2	1	0	0	1	1	0	1	0
3	0	1	0	1	1	0	1	0
4	1	0	1	0	0	1	1	0
5	0	1	1	0	0	1	1	0
6	1	0	0	1	0	1	1	0
7	0	1	0	1	0	1	1	0
8	1	0	1	0	0	1	0	1
9	0	1	0	1	0	1	0	1

Halt	0.33	HLT

When run button is depressed, continue with the next instruction.

No Operation	0.33	NOP

Execute the next instruction.

Clear	1.33	CLA ZEROs $\rightarrow (0_1)$

Store all ZEROs (fixed point binary ZERO) in the location specified by 0_1.

Store thin film	3.0	STF

The program address syllable 0_1 is a thin film register address. The contents of the specified thin film register is stored in the least significant end of the location specified by 0_2.

Load thin film	2.0	LTF

The program address syllable 0_2 is a thin film register address. The least significant portion of the contents of the location specified by 0_1 is stored in the specified thin film register.

Load Mask Register	0.33	LDM $(0_1) \rightarrow$ Mask Reg.

The least significant portion of the contents of the location specified by 0_1 is stored in the Mask Register.

Load Priority Register	0.33	LDP $(0_1) \rightarrow$ Priority Register

The least significant portion of the contents of the location specified by 0_1 is stored in the Priority Register.

Transmit	0.67	TRS $(0_1) \rightarrow 0_2$

The contents of the location specified by 0_1 is stored in 0_2.

Unconditional Transfer	1.67	UCT	0_1 + BPR	Program Counter

Take the next instruction from the address obtained by adding 0_1 to the Base Program Register (BPR).

Step Stack Up	0.33	SSU

Add ONE to the stack counter.

Step Stack Down	0.33	SSD

Subtract ONE from the stack counter.

Indexing Instructions

Increase Index	3.0	IXE, IXL

Increase the contents of the Index Register specified by 0_1 by the amount specified in 0_2. Compare the Index Register with the Limit Register specified by 0_1 for the condition indicated (E = equality, L = less than). If the condition is true, take the next instruction from the address specified by adding 0_3 to the Base Program Register (BPR). Otherwise, continue in sequence.

Decrease Index Register	DXE, DXG

Decrease the contents of the Index Register specified by 0_1 by the amount specified in 0_2. Compare the Index Register with the Limit Register specified by 0_1 for the condition indicated (E = equality, G = greater than). If the condition is true, take the next instruction from the address specified by adding 0_3 to the Base Program Register (BPR). Otherwise, continue in sequence.

Repeat	RPT

The 0_1 syllable is the repeat count. Syllable 0_2 contains three 4-bit address increments. Syllable 0_3 is a branch syllable. The repeated instruction is fetched from location 0_3 + BPR. The Repeat instruction and the first execution

of the repeated instruction employ normal address modification. The effective addresses of the first execution are retained. For subsequent iterations these addresses are incremented by the 0_2 syllable of the Repeat instruction. The repeated instruction is executed the number of times called for by the repeat count unless a branch occurs in the repeated instruction. In this case, the branch is executed and the repeat instruction terminates. If the repeat count reaches zero, program control continues in normal sequence.

Character Search	7.0	CSE	

The contents of the location specified by 0_1 is compared for equality 6-bits at a time with the character contained in 0_2. If equality occurs, store the character count in a thin film register and take the next instruction from the location specified by 0_3 + BPR. If no equality occurs, continue in normal sequence. Compare for inequality is also available. This selection is made in the 0_2 syllable.

Mask and Merge	12.0	MAM	$(0_1) \cdot (M_1)$ V $(0_2) \cdot (M_2) \rightarrow 0_3$

Contents of location specified by 0_1 are ANDed bit-by-bit with the contents of the M_1 mask register (in TF). Contents of location specified by 0_2 are ANDed bit-by-bit with contents of M_2 mask register (TF). The resulting quantities are ORed bit-by-bit and the final result is stored in the location specified by 0_3.

Sub-routine Jump	5.0	SRJ	(BPR), (BAR), (PAC) + $1 \rightarrow 0_1$

Load (BPR) (BAR) and (PC) + 1 into a program accessible register and load the low order 16-bits of the main memory location whose address is equal to the sum of the (SAR) and the literal portion of the address syllable of the SRJ instruction into PC, BPR, and BAR.

Sub-routine Return	2.0	SRR	$(0_1) \rightarrow$ BRK, BAR, PC

Load the three 16-bit segments of the program specified 48-bit word into BPR, BAR, and PC.

I/O Instruction

Transmit to I/O	TIO	I/O Descriptor → I/O Control Module

Transmit the I/O descriptor in the memory location specified by 0_1 to the first available I/O Control Module. If no control module is available, take the next instruction from the address specified by adding 0_2 to the Base Program Register (BPR). Otherwise, continue in sequence.

SECTION IV

AUTOMATIC PROGRAMMING

The large scale command and control systems, for which the D825 is particularly suited, require unusually large numbers of operational programs to perform their functions. In order to meet the urgent schedules imposed by the user and provide means for changing programs simply and rapidly, powerful automatic programming languages are necessary to insure high programmer productivity. With the D825, a compiler system is supplied using ALGOL 60 as its source language. The compiler has been extended beyond the requirements of ALGOL 60 to also make it useful for data processing applications. The ALGOL 60 language provides the rules for combining identifiers and operators into expressions, which are further compounded into the operational units of the language called statements. These statements, supported by declarative information about the kind of data referred to by an identifier, are the computing instructions to the D825 and its compiler.

The D825 was designed to be compatible with up to date developments in compiler design. Powerful problem-oriented languages such as ALGOL and COBOL were examined, and features for straight-forward quick translation of source programs in these and similar languages were included in the design for the D825. In this way, the translation of a problem language into one which is operationally efficient was solved in part by adopting a machine language in which instructions and operands are combined in a logical manner compatible with the way expressions are formed in the source language. The technique of the stack was introduced to provide for automatic retention of operands and partial results, thus eliminating the necessity for redundant data handling, and relieving the compiler of the necessity for assigning and maintaining temporary addressing.

As an example, in previous machines, the expression F = (A+B· C) +D· E is first translated into a 3 address pseudo code such as:

$$D \times E \longrightarrow T_1$$

$$B \times C \longrightarrow T_2$$

$$A + T_2 \longrightarrow T_2$$

$$T_1 + T_2 \longrightarrow F$$

which is then operated on to eliminate unnecessary temporary storage of intermediate results, and then translated into single address instruction form:

```
CAD     D
MUL     E
STA     T1
CAD     B
MUL     C
ADD     A
ADD     T1
STA     F
```

The ALGOL translater for the D825 would directly translate such an expression in a single pass:

```
FMU mms, D    , E       , FMU mms
   B     , C    , FADsss, FADssm
   F     ..
```

where the subscript "m" indicates that the operand address is an explicit memory address and the subscript "s" that the operand address is the top of the stack.

It is evident then, that the D825 provides those machine features that make possible the use of problem oriented language compilers without sacrificing the operational efficiency of the running programs.

Additional source languages, if called for, can be accomodated by providing translators from that language to the extended ALGOL 60 of the D825.

SECTION V

BURROUGHS ORGANIZATION AND EXPERIENCE

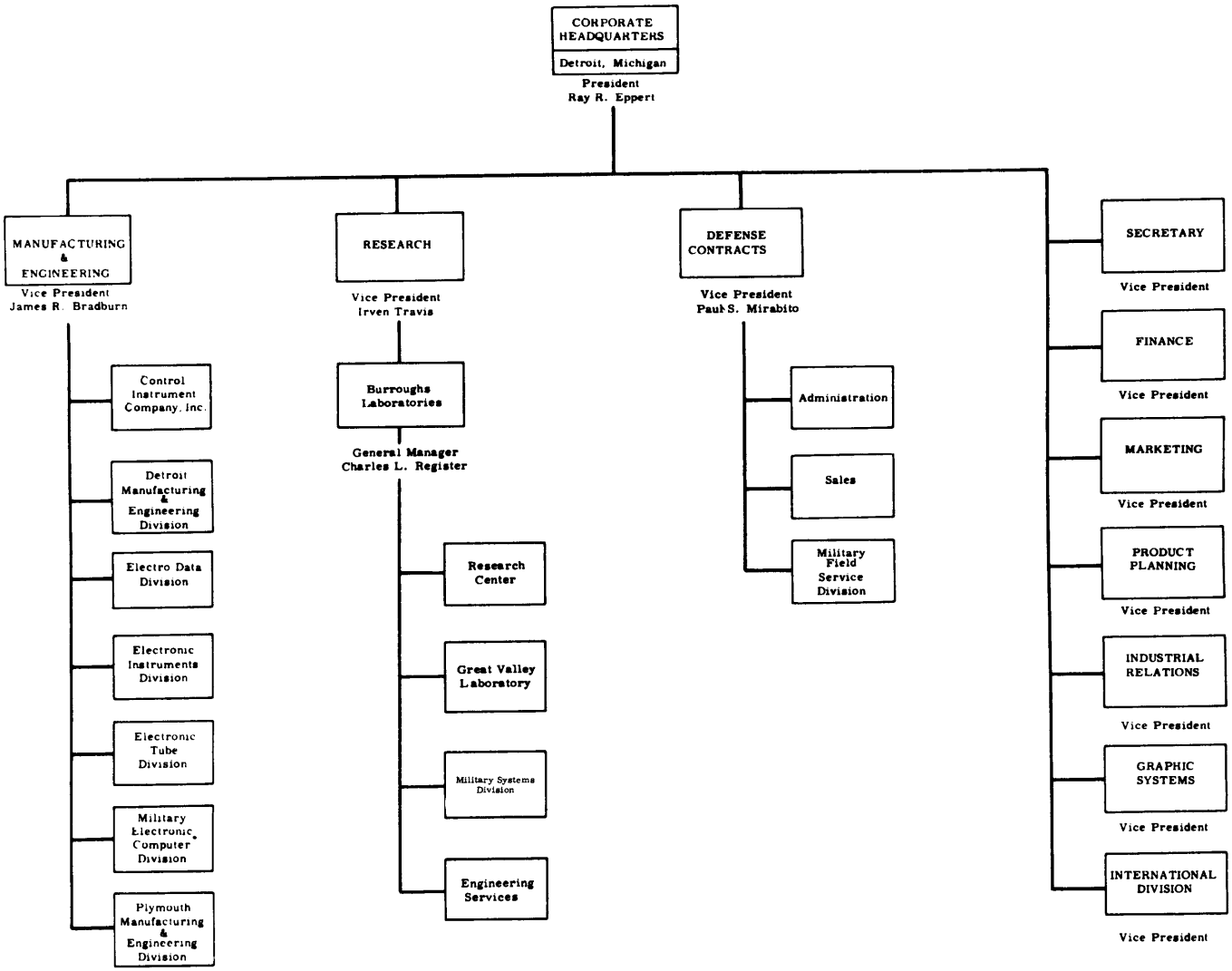
The Burroughs Corporation is a world wide engineering, manufacturing and marketing organization engaged principally in the creation and production of data-processing systems and allied equipments, systems, and materials. A recent series of achievements serve to indicate how the Burroughs tradename - traditionally identifiable with quality business machines and data processors - also embodies prestige in the production and systems management of large-scale military computation programs.

- 1954 - 1961 SAGE AN/FST-2 Data Processor development-production-installation-field support contract currently extending beyond $204 million expended for equipment now installed at 104 operational sites, marked by a record 99.4 percent around-the-clock availability performance. Initial delivery achieved within 15 months of contract award.

- 1955 - 1961 Atlas Ground Guidance Computer development-production-maintenance program for computer system which has participated in the guidance phase of approximately 75 long range missile flights and never failed or delayed the "count-down."

- 1959 - 1961 Airborne Long Range Input System Management of initial $35 million contract for expansion of the SAGE capability.

- 1960 - 1961 Polaris Submarine Stabilization Data Computer development-operational prototype-delivery achieved in less than the nine months allowed by contract.



Burroughs Corporate Organization

ENGINEERING ORGANIZATION AND FACILITIES

The Corporate organizational structure reflects the means by which Burroughs provides for an interchange of knowledge and production facilities to meet the diverse, but often similar, demands of the commercial and the military customer. Extensive facilities are closely integrated to perform the complete cycle of work for equipment programs: basic and applied research at the Research Center; research, development and prototype fabrication at Great Valley Laboratory; system management at the Military Systems Division; production in the Military Electronic Computer Division; and logistic support by the Military Field Service Division. These facilities -

- have sustained a variety of major programs, frequently under emergency schedules.
- permit performance in all important engineering areas at and beyond the state of the data processing art.
- include extensive Burroughs-developed automated computer assembly equipment.
- reflect a perfect record of labor peace throughout the 70-year Corporate history.
- provide field offices and logistics depots in many world-wide locations.

These facilities are immediately available for comprehensive performance.

Research Facilities

In Burroughs Laboratories at Paoli, Pennsylvania, military and commercial efforts complement each other in continuous quest for advancing the state-of-the-art in the field of electronic computation and data processing.

The Great Valley Laboratory is primarily engaged in military research and development projects. Here the engineering-scientific research team is supported by extensive facilities of 30 electronic laboratories located within its three modern buildings (104, 000 square feet).

The Research Center, containing 105, 000 square feet of working area, conducts basic and applied research over the broad field of data processing and performs development work primarily for commercial application in the fields of data acquisition, transmission, processing, storage, automatic recording, control, and display as applied to accounting, bankbookkeeping, industrial process control, office routines, and related programs. Research and development, for both military and commercial applications, of mechanical, electromechanical, electrostatic, and optical equipments in the data processing field are also conducted.

Facilities of the Research Center include an electrical and magnetic measurement laboratory, an applied physics laboratory, a metallographic microscopy laboratory, a metallurgical process laboratory, a chemical laboratory, a tube laboratory, and a printed circuit laboratory. These and other highly specialized facilities are available to all development programs at Great Valley Laboratory for the solution of detailed material or technique problems.

The Engineering Services plant, containing 40, 000 square feet of area, furnishes drafting, maintenance, instrument repair, shipping and receiving, and quality control services in support of Burroughs Laboratories.

The Military Systems Division, Air Force system manager for integration and development of SAGE long rang input equipment for RC-121 aircraft, is also located in Great Valley Laboratory and draws technological support from the Burroughs Laboratories.

The proximity of these facilities located within a three mile radius facilitates the interchange of scientific knowledge and engineering assignments in applying commercially developed techniques to military programs.

Production Facilities

Manufacturing facilities required for Burroughs military programs is provided by the Military Electronic Computer Division (MECD) in Detroit, which has approximately 185,000 square feet of floor space. Additional production support to MECD is provided by over 1,700,000 square feet of floor space in Burroughs other production facilities concentrated in the Detroit Area and on the East Coast. These production facilities are principally the Second Avenue Plant in Detroit, the Plymouth Plant in Plymouth, Michigan, the Control Instrument Company in Brooklyn, and the Electronic Instruments Division in Philadelphia.

MECD offers a completely integrated production facility which includes a printed circuit shop, automated dipsoldering equipment, and automatic component insertion equipment. Automatic package assembly equipment, developed by Burroughs and currently in use at MECD, is the most advanced in the industry. A skilled production team of over 3,000 personnel has already developed module fabrication techniques to a high degree of consistency on several large-scale, high-priority programs.

Field Service Facilities

Military related equipments manufactured by the Burroughs Corporation are installed and maintained by the Military Field Service Division (MFSD) which has its headquarters in two new modern buildings in Radnor, Pennsylvania. Currently some 1100 field engineers and skilled technicians are assigned to the field.

Logistics, engineering, technical manuals, and technical training departments of MFSD headquarters directly support field operation.

EXPERIENCE

Six principal military related product areas have evolved in the corporate effort: general purpose computing systems,

air defense systems, communications systems, airborne and naval systems, and ordnance fuzing and timing devices. The Corporation has advanced to a position of leadership in all five areas, conducting important large-scale programs, and performing system analysis and synthesis in each.

General Purpose Computing Systems

The experience gained by Burroughs in the development of the Burroughs 205 and 220 computing systems has most recently resulted in the Burroughs B5000 and D825 systems. The D825 is being designed and developed specifically for military related applications in a military environment. Both the D825 and B5000 are true parallel processing systems designed specifically to make efficient use of automatic programming techniques.

Missile Guidance Systems

Missile guidance system work commenced in 1955 with a contract for the development of the AN/GSQ-33 ground guidance computing system for the Atlas ICBM. Initial efforts involved extensive problem formulation and system integration study. The program to date has resulted in $100 million in contracts awarded to Burroughs.

Air Defense Systems

Effort in the air defense area begain in 1951 with a series of studies which led to a prototype development program for a large-scale digital computing system, the Multi-Weapon Automatic Target and Battery Evaluator (MATABE), for central control of the AN/GSG-2 point air defense system. This program was continued in a theoretical study, known as PADRE, of air defense strategy and tactics and system configuration and data processing specification for the post-1960 era. The extensive Burroughs effort in the SAGE air defense system begain in 1954 with a prototype development program for the AN/FST-2 Coordinate Data Transmitting Set. The success of the prototype led to an extensive expansion of the AN/FST-2 effort, including system analysis,

large-scale production, and logistic support. Burroughs SAGE experience and airborne systems capability led to the award of the ALRI system management contract initially funded at $35 million.

Communications Systems

Electronic communications equipment development in the Corporation begain in 1950 with contracts involving magnetic-core techniques, advanced logical design, and advanced cryptographic techniques. Many individual projects have been conducted in this area; the largest program includes contracts for several equipment types with a total value of more than $150 million. Equipments developed and produced by Burroughs in this field have demonstrated exceptional reliability, long life, low power consumption, and exceptional resistance to extreme environmental effects.

Airborne and Naval Systems

Burroughs airborne and naval systems efforts begain in 1950 with the production of the A-4 gun-bomb-rocket sight, and continued in 1952 with system management of the AN/ASB-1 Bomb Director System production and logistic support program. Two successful airborne computer programs for the U.S. Navy have been designed. One was for a general-purpose computer (NADAC) with outstanding speed, capacity, and flexibility, the second for an extremely compact muli-purpose computer with similar capabilities. The NADAC computer proved to be adaptable to a wide range of applications, which led to Contract Award for the Polaris Stabilization Data Computer. These computers are at the top state-of-the-art in high-performance airborne and naval computer design and high-density, high-reliability, packaging techniques.

Ordnance Timing and Fuzing Devices

Several development programs have been undertaken for the application of all-electronic timing and fuzing devices

to ordnance environments. In each of these programs, feasibility of the all-electronic ordnance timer has been demonstrated as a replacement for the inherently unreliable mechanical timer. This feasibility has been achieved by using the Bimag circuit (a Burroughs-developed bistable magnetic-core technique) and a magnetic systems engineering approach in the design of timing devices which must withstand temperature variations of 260°F, accelerations as high as 20,000g, and substantial nuclear radiations.

Other Devices and Systems

Burroughs has acquired invaluable experience in more specialized equipment areas, having performed important programs for a great variety of generally smaller electronic, electromechanical, and optical devices. Important technical advances have been made by Burroughs in the fields of printout, terminal equipment, optics, and recording techniques. Three important developments in this area are the large-scale, high-speed, specialized data-processing system, the world's fastest electrostatic output printers, and several major electro-optical devices for military use.

Related Study Programs

Burroughs-sponsored efforts have included such advanced system studies as the probabilistic machines, and high-speed computing methods. Additional areas of investigation have included DDA (Digital Differential Analyzer) development, high-speed circuit vehicles, modular packaging methods, reliability studies of components operating in a nuclear environment, and accelerated component life tests.

For the future, the Corporation looks forward to continued growth at a controlled rate affording new dimensions in computation for both military and commercial applications.

Burroughs Corporation

Detroit 32, Michigan

NEW DIMENSIONS / in computation for military systems